Data Sheet | December 21, 2006 | FN6221.0

Light-to-Digital Output Sensor with Address Selection, High Sensitivity, Gain Selection, Interrupt Function and I²C Interface

The ISL29004 is an integrated light sensor with a 16-bit integrating type ADC, I²C user programmable Lux range select for optimized counts/Lux, and I²C multi-function control and monitoring capabilities. The internal ADC provides 16-bit resolution while rejecting 50Hz and 60Hz flicker caused by artificial light sources.

In normal operation, power consumption is typically 300µA. Futhermore, an available software power-down mode controlled via the I²C interface reduces power consumption to less than 1µA. The device also support a hardware interrupt that remains asserted low until the host clears it through I²C interface.

The ISL29004 is in an 8 Ld ODFN package and has two I²C address pins for multiple devices on the same bus. The ISL29003 is a similar light sensor with a hardwired I²C address that is available in ODFN6 package.

Designed to operate on supplies from 2.5V to 3.3V, the ISL29004 are specified for operation over the -40°C to +85°C ambient temperature range.

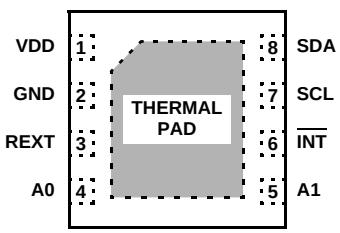
Ordering Information

PART NUMBER (Note)	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL29004IROZ	-	8 Ld ODFN	MDP0052
ISL29004IROZ-T7	7”	8 Ld ODFN Tape and Reel	MDP0052
ISL29004IROZ-EVALZ	Evaluation Board (Pb-free)		

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL29004
(8 LD ODFN)
TOP VIEW



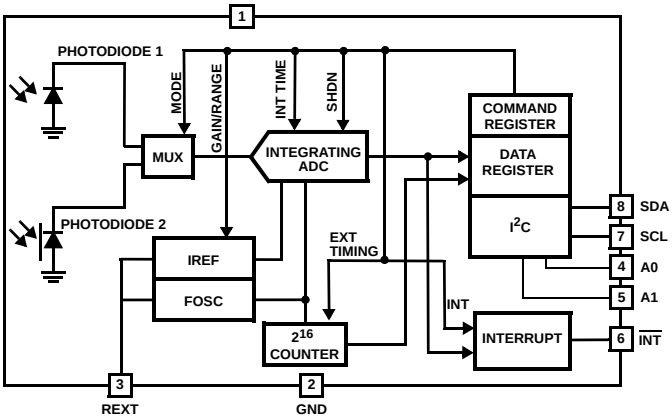
Features

- Range select via I²C
  - Range1 = 1000Lux
  - Range2 = 4000Lux
  - Range3 = 16,000Lux
  - Range4 = 64,000Lux
- Human eye response (540nm peak sensitivity)
- Temperature compensated
- 16-bit resolution
- Adjustable resolution: up to 65 counts per Lux
- User-programmable upper and lower threshold interrupt
- Simple output code, directly proportional to Lux
- 50Hz/60Hz rejection
- 2.5V to 3.3V supply
- 8 Ld ODFN (3mmx3mm)
- I²C address selection

Applications

- Ambient light sensing
- Backlight control
- Temperature control systems
- Contrast control
- Camera light meters
- Lighting controls

Block Diagram



ISL29004

Absolute Maximum Ratings (T_A = +25°C)

V_{DD} Supply Voltage between V_{DD} and GND 3.6V
I^2C Address Pin Voltage . . . . . -0.2V to 3.6
I^2C Bus Pin Voltage (SCL, SDA) . . . . . -0.2V to 5.5V
I^2C Bus Pin Current (SCL, SDA) . . . . . <10mA
R_{ext} Pin Voltage . . . . . -0.2V to 3.6V

Maximum Die Temperature . . . . . +125°C
Storage Temperature . . . . . -45°C to +100°C
Operating Temperature . . . . . -40°C to +85°C
ESD, Human Body Model 2kV
ESD, Machine Model 500V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{DD} = 3V, T_A = +25°C, R_{EXT} = 100kΩ 1% tolerance, unless otherwise specified, Internal Timing Mode operation (See Principles of Operation).

PARAMETER	DESCRIPTION	CONDITION		MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Range			2.25		3.63	V
I_{DD}	Supply Current				0.29	0.33	mA
I_{DD1}	Supply Current Disabled	Software disabled			0.1	1	µA
F_{OSC1}	Internal Oscillator Frequency	Gain/Range = 1 or 2		290	327	364	kHz
F_{OSC2}	Internal Oscillator Frequency	Gain/Range = 3 or 4		580	655	728	kHz
FI^2C	I^2C Clock Rate	(Note 2)		1		400	kHz
DATA0	Diode1 and Diode2 Dark ADC Code	E = 0Lux, Mode1, Gain/Range = 1			1	5	Counts
DATA1	Full Scale ADC Code					65535	Counts
DATA2	Diode1 ADC Code Gain/Range = 1 accuracy	Mode0	E = 300Lux, fluorescent light, Gain/Range = 1 (Note 1)	13,800	20,200	24,400	Counts
DATA3	Diode2 ADC Code Gain/Range = 1 accuracy	Mode1			2,020		Counts
DATA4	Diode1 ADC Code Gain/Range = 2 accuracy	Mode0	E = 300Lux, fluorescent light, Gain/Range = 2 (Note 1)		5,050		Counts
DATA5	Diode2 ADC Code Gain/Range = 2 accuracy	Mode1			505		Counts
DATA6	Diode1 ADC Code Gain/Range = 3 accuracy	Mode0	E = 300Lux, fluorescent light, Gain/Range = 3 (Note 1)		1,262		Counts
DATA7	Diode2 ADC Code Gain/Range = 3 accuracy	Mode1			126		Counts
DATA8	Diode1 ADC Code Gain/Range = 4 accuracy	Mode0	E = 300Lux, fluorescent light, Gain/Range = 4 (Note 1)		316		Counts
DATA9	Diode2 ADC Code Gain/Range = 4 accuracy	Mode1			32		Counts
V_{REF}	Voltage of R_{EXT} Pin				500		mV
V_{TL}	SCL, SDA, A0 and A1 Threshold LO	(Note 3)			1.05		V
V_{TH}	SCL and SDA Threshold HI	(Note 3)			1.95		V
I_{SDA}	SDA Current Sinking Capability			3	5		mA
$I_{\overline{INT}}$	$\overline{INT}$ Current Sinking Capability			3	5		mA
I_{IL}	A0 and A1 Input Current LO	A0 = A1 = GND			0.1		µA
I_{IH}	A0 and A1 Input Current HI	A0 = A1 = V_{DD}			0.1		µA

NOTES:

1. Fluorescent light is substituted by a white LED during production.
2. Minimum I^2C Clock Rate is guaranteed by design.
3. The voltage threshold levels of the SDA and SCL pins are VDD dependent: $V_{TL} = 0.35*V_{DD}$. $V_{TH} = 0.65*V_{DD}$.

Pin Descriptions

PIN NUMBER ISL29003	PIN NUMBER ISL29004	PIN NAME	DESCRIPTION	
1	1	VDD	Positive supply; connect this pin to a regulated 2.5V to 3.3V supply	
2	2	GND	Ground pin.	
3	3	REXT	External resistor pin for ADC reference; connect this pin to ground through a (nominal) 100kΩ resistor	
4	6	$\overline{INT}$	Interrupt pin; LO for interrupt/alarming. The $\overline{INT}$ pin is an open drain.	
5	7	SCL	I^2C serial clock	The I^2C bus lines can pulled above VDD, 5.5V max.
6	8	SDA	I^2C serial data	
N/A	4	A0	Bit 0 of the I^2C address.	The address pins have an open gate equivalent circuit. These are the least-significant bits of the I^2C address. The 4 possible addresses are 44(hex) through 47(hex).
N/A	5	A1	Bit 1 of the I^2C address.	

Principles of Operation

Photodiodes

The ISL29004 contain two photodiodes. Diode1 is sensitive to both visible and intrared light, while Diode2 is mostly sensitive to infrared light. The spectral response of the two diodes are independent from one another. See Figure Spectral Response vs Wavelength in the performance curves section. The photodiodes convert light to current. Then, the diodes' current outputs are converted to digital by a single built-in integrating type 16-bit Analog-to-Digital Converter (ADC). An I^2C command mode determines which photodiode will be converted to a digital signal. Mode0 is Diode1 only. Mode1 is Diode2 only. Mode3 is a sequential Mode0 and Mode1 with an internal subtract function (Diode1 - Diode2). Analog-to-Digital Converter.

The converter is a charge-balancing integrating type 16-bit ADC. The chosen method for conversion is best for converting small current signals in the presense of an AC periodic noise. A 100ms integration time, for instance, highly rejects 50Hz and 60Hz power line noise simultaneously. See Integration Time and Noise Rejection section.

The built-in ADC offers user flexibility in integration time or conversion time. Two timing modes are available. Internal Timing Mode and External Timing Mode. In Internal Timing Mode, integration time is determined by an internal dual speed oscillator (fosc), and the n-bit (n = 4, 8, 12,16) counter inside the ADC. In External Timing Mode, integration time is determined by the time between two consecutive I^2C External Timing Mode commands. See External Timing Mode example. A good balancing act of integration time and resolution depending on the application is required for optimal results.

The ADC has four I^2C programmable range select to dynamically accomodate various lighting conditions. For very dim conditions, the ADC can be configured at its lowest range. For very bright conditions, the ADC can be configured at its highest range.

Interrupt Function

The active low interrupt pin is an open drain pull-down configuration. The interrput pin serves as an alarm or monitoring function to determine whether the ambient light exceeds the upper threshold or goes below the lower threshold. The user can also configure the persistency of the interrupt pin. This eliminates any false triggers such as noise or sudden spikes in ambient light conditions. An unexpected camera flash for example can be ignored by setting the persistency to 8 integration cycles.

I^2C Interface

There are eight (8) 8-bit registers available inside the ISL29004. The command and control registers define the operation of the device. The command and control registers do not change until the registers are overwritten.There are two 8-bit registers that set the high and low interrupt thresholds. There are four 8-bit data Read Only registers. Two bytes for the sensor reading and another two bytes for the timer counts. The data registers contain the ADC's latest digital output, and the number of clock cycles in the previous integration period.

The ISL29004's I^2C interface slave address is pin-selectable by pins A0 and A1. These pins can be tied or driven either high or low. They comprise the least-significant two bits of the I^2C address, while the 5 most-significant bits are hardwired as 100001{A1}{A0}. The four possible addresses are therefore 44(hex) through 47(hex).

The ISL29003's I^2C interface slave address is hardwired internally as 44(hex).

Figure 1 shows a sample one-byte read. Figure 2 shows a sample one-byte write. Figure 3 shows a sync_iic timing diagram sample for externally controlled integration time. The I^2C bus master always drives the SCL (clock) line, while either the master or the slave can drive the SDA (data) line. Every I^2C transaction begins with the master asserting a start condition (SDA falling while SCL remains high). The following byte is driven by the master, and includes the slave address and read/write bit. The receiving device is responsible for pulling SDA low during the acknowledgement period.

Every I^2C transaction ends with the master asserting a stop condition (SDA rising while SCL remains high).

For more information about the I^2C standard, please consult the Philips® I^2C specification documents.

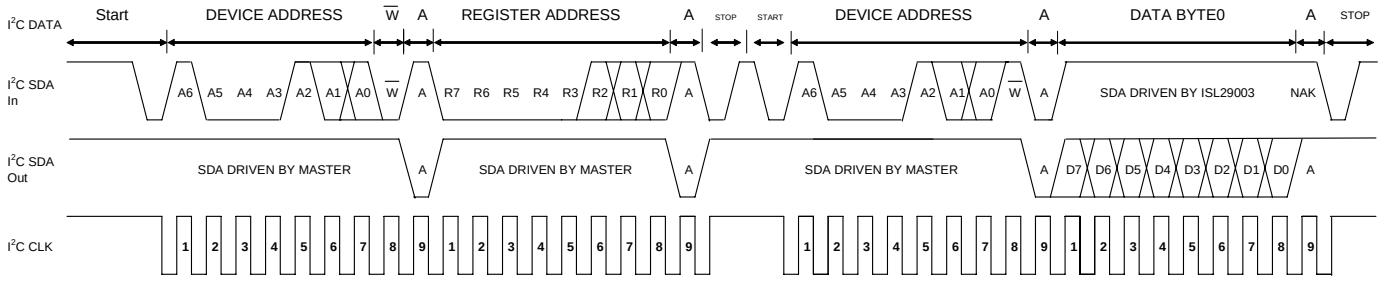


FIGURE 1. I²C READ TIMING DIAGRAM SAMPLE

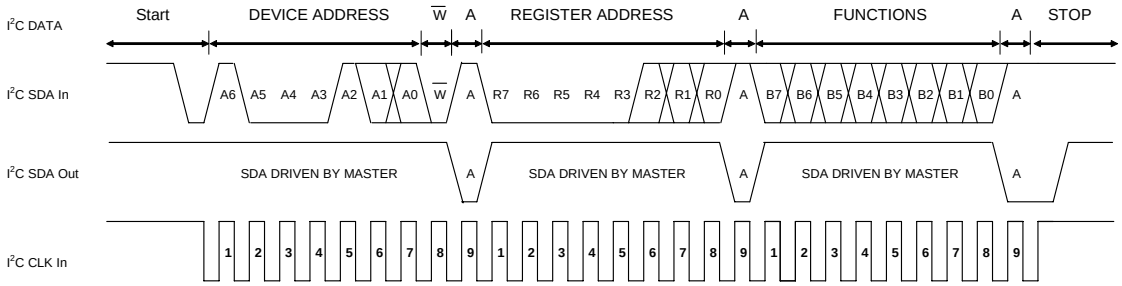


FIGURE 2. I²C WRITE TIMING DIAGRAM SAMPLE

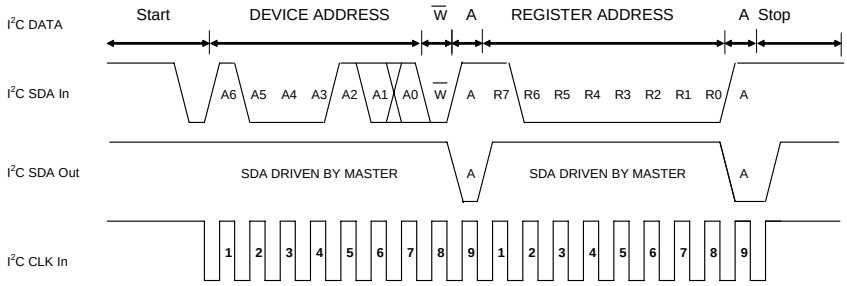


FIGURE 3. I²C sync_iic TIMING DIAGRAM SAMPLE

Register Set

There are eight registers that are available in the ISL29004. Table 1 summarizes the available registers and their functions.

TABLE 1. REGISTER SET

ADDR (HEX)	REGISTER NAME	Bit(s)	FUNCTION NAME	FUNCTIONS/DESCRIPTION
00	Command	7	enable	0: disable adc-core 1: enable adc-core
		6	adcPD	0: Normal operation 1: Power Down Mode
		5	Timing_Mode	0: Integration is internally timed 1: Integration is externally sync/controlled by I^2C host
		4	reserved	
		3:2	mode<1:0>	Selects ADC work mode 0: Diode1's current to unsigned 16-bit data 1: Diode2's current to unsigned 16-bit data 2: Difference between diodes (I1 - I2) to signed 15-bit data 3: reserved
		1:0	width<1:0>	number of clock cycles; n-bit resolution 0: 2^{16} cycles 1: 2^{12} cycles 2: 2^{8} cycles 3: 2^{4} cycles
01	Control	7	ext_mode	Always set to logic 0. Factory use only.
		6	test_mode	Always set to logic 0
		5	int_flag	0: Interrupt is cleared or not yet triggered 1: Interrupt is triggered
		4	reserved	Always set to logic 0. Factory use only.
		3:2	gain<1:0>	Selects the gain so range is 0: 0 - 1000Lux 1: 0 - 4000Lux 2: 0 - 16000Lux 3: 0 - 64000Lux
		1:0	int_persist <1:0>	Interrupt is triggered after 0: 1 integration cycle 1: 4 integration cycles 2: 8 integration cycles 3: 16 integration cycles
02	Interrupt threshold HI	7:0	Interrupt threshold HI	High byte of HI interrupt threshold. Default is 0xFF
03	Interrupt threshold LO	7:0	Interrupt threshold LO	High byte of the LO interrupt threshold. Default is 0x00
04	LSB_sensor	7:0	LSB_sensor	Read-Only data register that contains the least significant byte of the latest sensor reading
05	MSB_sensor	7:0	MSB_sensor	Read-Only data register that contains the most significant byte of the latest sensor reading
06	LSB_timer	7:0	LSB_timer	Read-Only data register that contains the least significant byte of the timer counter value corresponding to the latest sensor reading.
07	MSB_timer	7:0	MSB_timer	Read-Only data register that contains the most significant byte of the timer counter value corresponding to the latest sensor reading.

TABLE 2. WRITE ONLY REGISTERS

ADDRESS	REGISTER NAME	FUNCTIONS/ DESCRIPTION
b1xxx_xxxx	sync_iic	Writing a logic 1 to this address bit ends the current adc-integration and starts another. Used only with External Timing Mode.
bx1xx_xxxx	clar_int	Writing a logic 1 to this address bit clears the interrupt.

Command Register 00(hex)

The Read/Write command register has five functions:

(1) Enable; Bit 7.This function either resets the ADC or enables the ADC in normal operation. A logic 0 disables ADC to reset-mode. A logic 1 enables adc to normal operation.

TABLE 3. ENABLE

BIT 7	OPERATION
0	Disable ADC-core to reset-mode (default)
1	Enable ADC-core to normal operation

(2) AdcPD; Bit 6. This function puts the device in a power down mode. A logic 0 puts the device in normal operation. A logic 1 powers down the device.

TABLE 4. adcPD

BIT 6	OPERATION
0	Normal operation (default)
1	Power Down

(3) Timing Mode; Bit 5. This function determines whether the integration time is done internally or externally. In Internal Timing Mode, integration time is determined by an internal dual speed oscillator (fosc), and the n-bit (n = 4, 8, 12,16) counter inside the ADC. In External Timing Mode, integration time is determined by the time between two consecutive external-sync sync_iic pules commands.

TABLE 5. TIMING MODE

BIT 5	OPERATION
0	Internal Timing Mode. Integration time is internally timed determined by fosc, REXT, and number of clock cycles.
1	External Timing Mode. Integration time is externally timed by the I2C host.

(4) Photodiode Select Mode; Bits 3 and 2. This function controls the mux attached to the two photodiodes. At Mode0, the mux directs the current of Diode1 to the ADC. At Mode1, the mux directs the current of Diode2 only to the ADC. Mode3 is a sequential Mode0 and Mode1 with an internal subtract function (Diode1 - Diode2).

TABLE 6. PHOTODIODE SELECT MODE; BITS 2 AND 3

BITS 3:2	MODE
0:0	Mode0. ADC integrates or converts Diode1 only. Current is converted to an n-bit unsigned data.*
0:1	Mode1. ADC integrates or coverts Diode2 only. Current is converted to an n-bit unsigned data.*
1:0	MODE3. A sequential Mode0 then Mode1 operation. The difference current is an (n-1) signed data.*
1:1	No operation.

* n = 4, 8, 12,16 depending on the number of clock cycles function.

(5) Width; Bits 1 and 0. This function determines the number of clock cycles per conversion. Changing the number of clock cycles does more than just change the resolution of the device. It also changes the integration time, which is the period the device's analog-to-digital (A/D) converter samples the photodiode current signal for a Lux measurement.

TABLE 7. WIDTH

BITS 1:0	NUMBER OF CLOCK CYCLES
0:0	2^16 = 65,536
0:1	2^12 = 4,096
1:0	2^8 = 256
1:1	2^4 = 16

Control Register 01(hex)

The Read/Write control register has three functions:

(1) Interrupt flag; Bit 5. This is the status bit of the interrupt. The bit is set to logic high when the interrupt thresholds have been triggered, and logic low when not yet triggered. Writing a logic low clears/resets the status bit.

TABLE 8. INTERRUPT FLAG

BIT 5	OPERATION
0	Interrupt is cleared or not triggered yet
1	Interrupt is triggered

(2) Range/Gain; Bits 3 and 2. The Full Scale Range can be adjusted by an external resistor Rext and/or it can be adjusted via I2C using the Gain/Range funtion. Gain/Range has four possible values, Range(k) where k is 1 through 4. Table 9 lists the possible values of Range(k) and the resulting FSR for some typical value R_{EXT} resistors. When Gain/Range is set to Range1 or Range2, the fosc runs at 327kHz. When Gain/Range is set to Range3 or Range4 fosc runs at twice the rate at 655kHz. The automatic fosc adjustment feature improves signal-to-noise ratio for low Lux measurements.

TABLE 9. RANGE/GAIN TYPICAL FSR LUX RANGES

BITS 3:2	k	RANGE(k)	FSR LUX RANGE@ R_{EXT} = 100k	FSR LUX RANGE@ R_{EXT} = 50k	FSR LUX RANGE@ R_{EXT} = 500k
0:0	1	973	973	1946	195
0:1	2	3892	3892	7784	778
1:0	3	15,568	15,568	31,136	3114
1:1	4	62,272	62,272	124,544	12,454

Interrupt persist; Bits 1 and 0. The interrupt pin and the interrupt flag is triggered/set when the data sensor reading is out of the interrupt threshold window after m consecutive number of integration cycles. The interrupt persist bits determine m.

TABLE 10. INTERRUPT PERSIST

BITS 1:0	NUMBER OF INTEGRATION CYCLES
0:0	1
0:1	4
1:0	8
1:1	16

Interrupt Threshold HI Register 02(hex)

This register sets the the HI threshold for the interrupt pin and the interrupt flag. By default the Interrupt threshold HI is FF(hex). The 8-bit data written to the register represents the upper MSB of a 16-bit value. The LSB is always 00(hex).

Interrupt Threshold LO Register 03(hex)

This register sets the the LO threshold for the interrupt pin and the interrupt flag. By default the Interrupt threshold LO is 00(hex). The 8-bit data written to the register represents the upper MSB of a 16-bit value. The LSB is always 00(hex).

Sensor Data Register 04(hex) and 05(hex)

When the device is configured to output a 16-bit data, the most significant byte is accessed at 04(hex), and the least significant byte can be accessed at 05(hex). The sensor data register is refreshed after very integration cycle.

Timer Data Register 06(hex) and 07(hex)

Note that the timer counter value is only available when using the External Timing Mode. The 06(hex) and 07(hex) are the LSB and MSB respectively of a 16-bit timer counter value corresponding to the most recent sensor reading. Each clock cycle increments the counter. At the end of each integration period, the value of this counter is made available over the I^2C. This value can be used to eliminate noise introduced by slight timing errors caused by imprecise external timing. Microcontrollers, for example, often cannot provide high-accuracy command-to-command timing, and the timer counter value can be used to eliminate the resulting noise.

TABLE 11. DATA REGISTERS

ADDRESS (hex)	CONTENTS
04	Least-significant byte of most recent sensor reading.
05	Most-significant byte of most recent sensor reading.
06	Least-significant byte of timer counter value corresponding to most recent sensor reading.
07	Most-significant byte of timer counter value corresponding to most recent sensor reading.

Calculating Lux

The ISL29004's output codes, DATA, are directly proportional to Lux.

$$E = \alpha \times DATA \quad \text{(EQ. 1)}$$

The proportionality constant α is determined by the Full Scale Range, FSR, and the n-bit ADC which is user defined in the command register. The proportionality constant can also be viewed as the resolution; The smallest Lux measurement the device can measure is α.

$$\alpha = \frac{FSR}{2^n} \quad \text{(EQ. 2)}$$

Full Scale Range, FSR, is determined by the software programmable Range/Gain, Range(k), in the command register and an external scaling resistor R_{EXT} which is referenced to 100kΩ.

$$FSR = Range(k) \times \frac{100k\Omega}{R_{EXT}} \quad \text{(EQ. 3)}$$

The transfer function effectively for each timing mode becomes:

INTERNAL TIMING MODE

$$E = \frac{Range(k) \times \frac{100k\Omega}{R_{EXT}}}{2^n} \times DATA \quad \text{(EQ. 4)}$$

EXTERNAL TIMING MODE

$$E = \frac{Range(k) \times \frac{100k\Omega}{R_{EXT}}}{COUNTER} \times DATA \quad \text{(EQ. 5)}$$

n = 4, 8, 12, or 16. This is the number of clock cycles programmed in the command register.

Range(k) is the user defined range in the Gain/Range bit in the command register.

R_{EXT} is an external scaling resistor hardwired to the R_{EXT} pin.

DATA is the output sensor reading in number of counts available at the data register.

2^n represents the maximum number of counts possible in Internal Timing Mode. For the External Timing Mode the

maximum number of counts is stored in the data register named COUNTER

COUNTER is the number increments accrued for between integration time for External Timing Mode.

Gain/Range, Range(k)

The Gain/Range can be programmed in the control register to give Range (k) determining the FSR. Note that Range(k) is not the FSR. See Equation 3. Range(k) provides four constants depending on programmed k that will be scaled by R_{EXT}. See Table 9. Unlike R_{EXT}, Range(k) dynamically adjusts the FSR. This function is especially useful when light conditions are varying drastically while maintaining excellent resolution.

Number of Clock Cycles, n-bit ADC

The number of clock cycles determines “n” in the n-bit ADC; 2^n clock cycles is a n-bit ADC. n is programmable in the command register in the width function. Depending on the application, a good balance of speed, and resolution has to be considered when deciding for n. For fast and quick measurement, choose the smallest n = 4. For maximum resolution without regard of time, choose n = 16. Table 12 compares the tradeoff between integration time and resolution. See Equations 10 and 11 for the relation between integration time and n. See Equation 3 for the relation of n and resolution.

TABLE 12. RESOLUTION AND INTEGRATION TIME SELECTION

	RANGE1 fosc = 327kHz		RANGE4 fosc = 655kHz	
n	TINT (ms)	RESOLUTION LUX/COUNT	TINT (ms)	RESOLUTION (LUX/COUNT)
16	200	0.01	100	1
12	12.8	0.24	6.4	16
8	0.8	3.90	0.4	250
4	0.05	62.5	0.025	4000

R_{EXT} = 100kΩ

External Scaling Resistor R_{EXT} and f_{osc}

The ISL29004 use an external resistor R_{EXT} to fix its internal oscillator frequency, f_{osc}. Consequently, R_{EXT} determines the fosc, integration time and the FSR of the device. Fosc, a dual speed mode oscillator, is inversely proportional to R_{EXT}. For user simplicity, the proportionality constant is referenced to fixed constants 100kΩ and 655kHz:

$$fosc1 = \frac{1}{2} \times \frac{100k\Omega}{R_{EXT}} \times 655kHz \quad \text{(EQ. 6)}$$

$$fosc2 = \frac{100k\Omega}{R_{EXT}} \times 655kHz \quad \text{(EQ. 7)}$$

fosc1 is oscillator frequency when Range1 or Range2 are set. This is nominally 327kHz when R_{EXT} is 100kΩ.

fosc2 is the oscillator frequency when Range3 or Range4 are set. This is nominally 655kHz when R_{EXT} is 100kΩ.

When the Range/Gain bits are set to Range1 or Range2, fosc runs at half speed comapred to when Range/Gain bits are set to Range3 and Range4.

$$f_{osc}1 = \frac{1}{2}(f_{osc}2) \quad \text{(EQ. 8)}$$

The automatic fosc adjustment feature allows significant improvement of signal-to-noise ratio when detecting very low Lux signals.

Integration Time or Conversion Time

Integration time is the period during which the device’s analog-to-digital ADC converter samples the photodiode current signal for a Lux measurement. Integration time, in other words, is the time to complete the conversion of analog photodiode current into a digital signal-number of counts.

Integration time affects the measurement resolution. For better resolution, use a longer integration time. For short and fast conversions use a shorter integration time.

The ISL29004 offer user flexibility in the integration time to balance resolution, speed and noise rejection. Integration time can be set internally or externally and can be programmed in the command register 00(hex) bit 5.

INTEGRATION TIME IN INTERNAL TIMING MODE

This timing mode is programmed in the command register 00(hex) bit 5. Most applications will be using this timing mode. When using the Internal Timing Mode, f_{osc} and n-bits resolution determine the integration time. T_{int} is a function of the number of clock cycles and fosc.

$$T_{int} = 2^n \times \frac{1}{f_{osc}} \quad \text{For Internal Timing Mode Only} \quad \text{(EQ. 9)}$$

n = 4, 8, 12, and16. n is the number of bits of resolution.

2^n therefore is the number of clock cycles. n can be programmed at the command register 00(hex) bits 1 and 0.

Since fosc is dual speed depending on the Gain/Range bit, T_{int} is dual time. The integration time as a function of R_{EXT} and n is:

$$T_{int}1 = 2^n \times \frac{R_{EXT}}{327kHz \times 100k\Omega} \quad \text{(EQ. 10)}$$

T_{int1} is the integration time when the the device is configured for Internal Timing Mode and Gain/Range is set to Range1 or Range2.

$$T_{int}2 = 2^n \times \frac{R_{EXT}}{655kHz \times 100k\Omega} \quad \text{(EQ. 11)}$$

T_{int2} is the integration time when the the device is configured for Internal Timing Mode and Gain/Range is set to Range3 or Range4.

TABLE 13. INTEGRATION TIMES FOR TYPICAL R_{EXT} VALUES

R_{EXT} (kΩ)	RANGE1 RANGE2		RANGE3 RANGE4	
	n = 16-BIT	n = 12-BIT	n = 12-BIT	n = 4
50	100	6.4	13	0.013
100**	**200**	**13**	**26**	**0.025**
200	400	26	52	0.050
500	1000	64	128	0.125

*Integration time in milliseconds
**Recommended R_{EXT} resistor value

INTEGRATION TIME IN EXTERNAL TIMING MODE

This timing mode is programmed in the command register 00(hex) bit 5. External Timing Mode is recommended when integration time can be synchronized to an external signal such as a PWM to eliminate noise.

For Mode0 or Mode1 operation, the integration starts when the sync_iic command is sent over the I^2C lines. The device needs two sync_iic commands to complete a photodiode conversion. The integration then stops when another sync_iic command is received. Writing a logic 1 to the sync_iic bit ends the current adc integration and starts another one.

For Mode3, the operation is a sequential Mode0 and Mode1. The device needs three sync_iic commands to complete two photodiode measurments. The 1st sync_iic command starts the conversion of the diode1. The 2nd sync_iic completes the conversion of diode1 and starts the conversion of diode2. The 3rd sync_iic pules ends the conversion of diode2 and starts over again to commence conversion of diode1.

The integration time, T_{int}, is determined by the following equation:

$$T_{int} = \frac{i_{I2C}}{f_{I2C}} \quad \text{(EQ. 12)}$$

i_{I2C} is the number of I^2C clock cycles to obtain the T_{int}.
f_{I2C} is the I^2C operating frequency

The internal oscillator, f_{OSC}, operates identically in both the internal and external timing modes, with the same dependence on R_{EXT}. However, in External Timing Mode, the number of clock cycles per integration is no longer fixed at 2^n. The number of clock cycles varies with the chosen integration time, and is limited to 2^{16} = 65,536. In order to avoid erroneous Lux readings the integration time must be short enough not to allow an overflow in the counter register.

$$T_{int} < \frac{65,535}{f_{OSC}} \quad \text{(EQ. 13)}$$

f_{osc} = 327kHz*100kΩ/R_{EXT}. When Range/Gain is set to Range1 or Range2.

f_{osc} = 655kHz*100kΩ/R_{EXT}. When Range/Gain is set to Range3 or Range4.

Noise Rejection

In general, integrating type ADC's have an excellent noise-rejection characteristics for periodic noise sources whose frequency is an integer multiple of the integration time. For instance, a 60Hz AC unwanted signal's sum from 0ms to k*16.66ms (k = 1,2...k_i) is zero. Similarly, setting the device's integration time to be an integer multiple of the periodic noise signal, greatly improves the light sensor output signal in the presence of noise.

Design Example 1

The ISl29004 will be designed in a portable system. The ambient light conditions that the device will be exposed to is at most 500Lux which is a good office lighting. The light source has a 50/60Hz power line noise which is not visible by the human eye. The I2C clock is 10kHz.

Solution 1 - Using Internal Timing Mode

In order to achieve both 60Hz and 50Hz AC noise rejection, the integration time needs to be adjusted to coincide with an integer multiple of the AC noise cycle times.

T_{int} = i(1/60Hz) = j(1/50Hz).

The first instance of integer values at which T_{int} rejects both 60Hz and 50Hz is when i = 6, and j= 5.

T_{int} = 6(1/60Hz) = 5(1/50Hz)

T_{int} = 100ms

Next, the Gain/Range needs to be determined. Based on the application condition given, Lux(max) = 500Lux, a range of 1000Lux is desirable. This corresponds to a Gain/Range Range1 mode. Also impose a resolution of n = 16-bit. Hence we choose equation 10 to determine R_{EXT}.

$$R_{EXT} = \frac{T_{int} \times 327kHz \times 100k\Omega}{2^n} \quad \text{(EQ. 14)}$$

R_{EXT} = 50kΩ

for Internal Timing Mode and Gain/Range is set to Range3 or Range

The Full Scale Range, FSR, needs to be determined. From Equation 3:

$$FSR = 1000Lux\frac{100k\Omega}{50k\Omega}$$

$$\mathbf{FSR = 2000Lux}$$

The effective transfer function becomes:

$$\mathbf{E = \frac{data}{2^{16}} \times 2000Lux}$$

TABLE 14. SOLUTION1 SUMMARY TO EXAMPLE DESIGN PROBLEM

DESIGN PARAMETER	VALUE
T_{int}	100ms
R_{EXT}	50kΩ
Gain/Range Mode	Range1 = 1000Lux
FSR	2000Lux
# of clock cycles	2^{16}
Transfer Function	$E = \frac{DATA}{2^{16}} \times 2000Lux$

Solution 2 - Using External Timing Mode

From solution 1, the desired integration time is 100ms. Note that the R_{EXT} resistor only determines the inter oscillator frequency when using external timing mode. Instead the integration time is the time between two sync_iic commands sent through the I^2C. The programmer determines how many I^2C clock cycles to wait between two external timing commands.

$i_{I2C} = f_{I2C} * T_{int}$ = number of I^2C clock cycles

i_{I2C} = 10kHz *100ms

i_{I2C} = 1,000 I^2C clock cycles. An external sync_iic command sent 1,000 cycles after another sync_iic command rejects both 60Hz and 50Hz AC noise signals.

Next is to pick an arbitrary R_{EXT} = 100kΩ and to choose the Gain/Range Mode. For a maximum 500Lux, Range1 is adequate. From Equation 3:

$$FSR = 1000lux\frac{100k\Omega}{100k\Omega}$$

$$\mathbf{FSR = 1000Lux}$$

The effective transfer function becomes:

$$\mathbf{E = \frac{DATA}{COUNTER} \times 1000Lux}$$

DATA is the sensor reading data located in data registers 04(hex) and 05(hex)

COUNTER is the timer counter value data located in data registers 06(hex) and 07(hex). In this sample problem, COUNTER = 1000.

TABLE 15. SOLUTION2 SUMMARY TO EXAMPLE DESIGN PROBLEM

DESIGN PARAMETER	VALUE
T_{int}	100ms
R_{EXT}	100kΩ
Gain/Range Mode	Range1 = 1000Lux
FSR	1000Lux
# of clock cycles	COUNTER = 1000
Transfer Function	$E = \frac{DATA}{COUNTER} \times 1000Lux$

Light Source Detection and Infra-Red Rejection

Any filament type light source has a high presence of infrared component invisible to the human eye. A white fluorescent lamp, on the other hand has a low IR content. As a result, output sensitivity may vary depending on the light source. Maximum attenuation of IR can be achieved by properly scaling the readings of Diode1 and Diode2. The user obtains data reading from sensor diode 1, D1, which is sensitive to visible and IR, then reading from sensor diode 2, D2 which is mostly sensitive from IR. The graph on Figure 7 shows the effective spectral response after applying Equation 15 of the ISL29003 from 400nm to 1000nm. The equation below describes the method of cancelling IR in internal timing mode.

$$D3 = n(D1 - kD2) \quad \text{(EQ. 15)}$$

Where:

D3 = Lux amount in number of counts less IR presence

D1 = data reading of Diode 1

D2 = data reading of Diode 2

n = 1.355. This is a fudge factor to scale back the sensitivity up to ensure Equation 4 is valid.

k = 3.355. This is a scaling factor for the IR sensitive Diode 2.

Flat Window Lens Design

A window lens will surely limit the viewing angle of the ISL29004. The window lens should be placed directly on top of the device. The thickness of the lens should be kept at minimum to minimize loss of power due to reflection and also to minimize loss of loss due to absorption of energy in the plastic material. A thickness of t = 1mm is recommended for a window lens design. The bigger the diameter of the window lens the wider the viewing angle is of the ISL29001. Table 16 shows the recommended dimensions of the optical window to ensure both +35° and +45° viewing angle. These

dimensions are based on a window lens thickness of 1.0mm and a refractive index of 1.59.

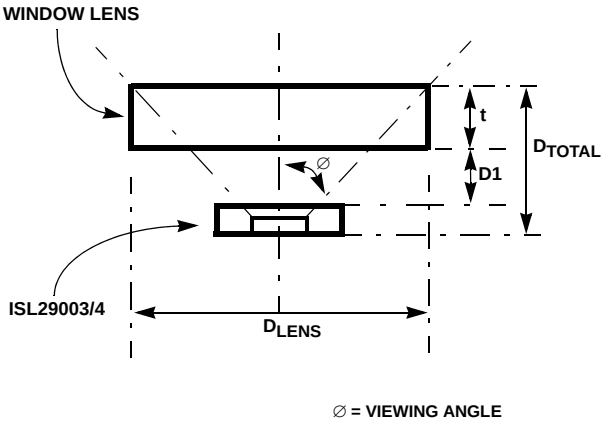


FIGURE 4. FLAT WINDOW LENS

TABLE 16. RECOMMENDED DIMENSIONS FOR A FLAT WINDOW DESIGN

D_{TOTAL}	D1	D_{LENS} @ 35 VIEWING ANGLE	D_{LENS} @ 45 VIEWING ANGLE
1.5	0.50	2.25	3.75
2.0	1.00	3.00	4.75
2.5	1.50	3.75	5.75
3.0	2.00	4.30	6.75
3.5	2.50	5.00	7.75

t = 1	Thickness of lens
D1	Distance between ISL29001 and inner edge of lens
D_{LENS}	Diameter of lens
D_{TOTAL}	Distance constraint between the ISL29001 and lens outer edge

* All dimensions are in mm.

Window with Light Guide Design

If a smaller window is desired while maintaining a wide effective viewing angle of the ISL29004, a cylindrical piece of transparent plastic is needed to trap the light and then focus and guide the light on to the device. Hence the name light guide or also known as light pipe. The pipe should be placed directly on top of the device with a distance of D1 = 0.5mm to achieve peak performance. The light pipe should have minimum of 1.5mm in diameter to ensure that whole area of the sensor will be exposed. See Figure 5.

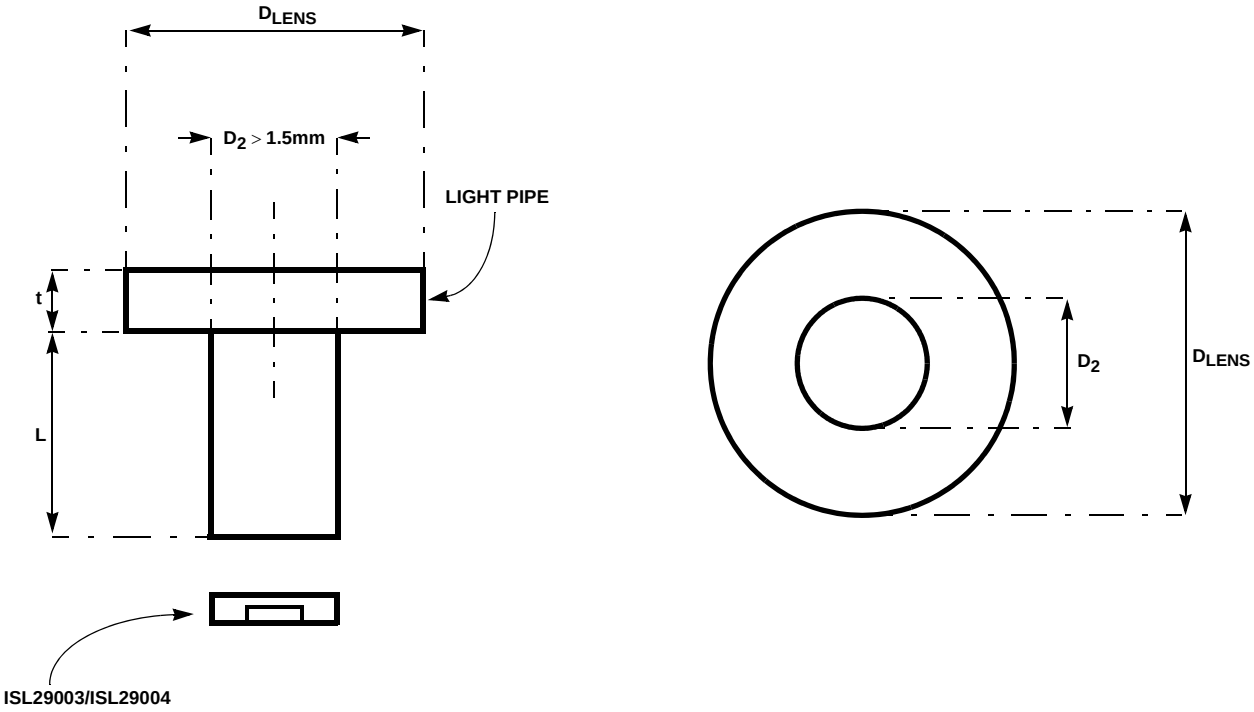
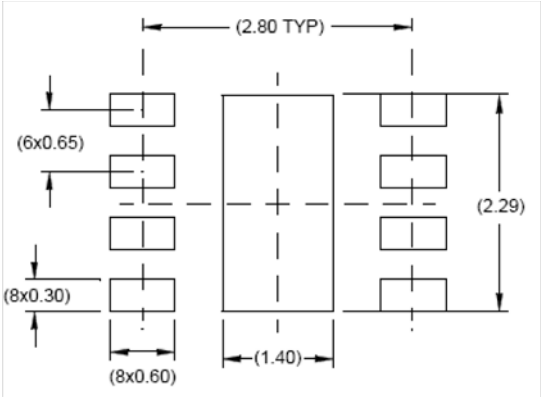


FIGURE 5. WINDOW WITH LIGHT GUIDE/PIPE



Dimensions in mm

FIGURE 6. SUGGESTED PCB FOOTPRINT

Suggested PCB Footprint

Footprint pads should be a nominal 1-to-1 correspondence with package pads. The large exposed central die-mounting paddle in the center of the package has no electrical connection. It is, however, recommended to have the thermal pad soldered to GND for package reliability.

Layout Considerations

The ISL29004 is relatively insensitive to layout. Like other I^2C devices, it is intended to provide excellent performance even in significantly noisy environments. There are only a few considerations that will ensure best performance.

Route the supply and I^2C traces as far as possible from all sources of noise. Use two power-supply decoupling capacitors, 4.7µF and 0.1µF, placed close to the device.

Typical Circuit

A typical application for the ISL29004 is shown in Figure 7. Additional I^2C address select pins A0 and A1 are available for the ISL29004 so a maximum of four ISL29004 devices can be tied on the same I^2C bus line.

Soldering Considerations

Convection heating is recommended for reflow soldering; direct-infrared heating is not recommended. The ISL29004's plastic ODFN package does not require a custom reflow soldering profile, and is qualified up to +260°C. A standard reflow soldering profile with a +260°C maximum is recommended.

Special Handling

ODFN8 is rated as JEDEC moisture level 4. Standard JEDEC Level 4 procedure should be followed: 72hr floor life at less than +30°C 60% RH. When baking the device, the temperature required is +110°C or less due to its special molding compound.

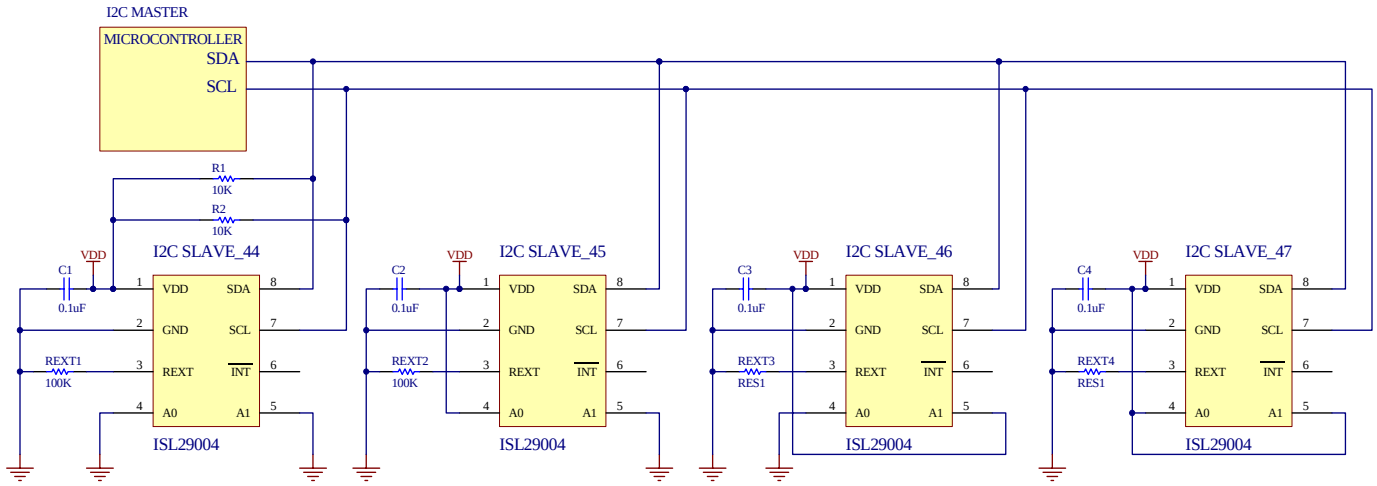


FIGURE 7. ISL29004 TYPICAL CIRCUIT

Typical Performance Curves (R_{EXT} = 100kΩ)

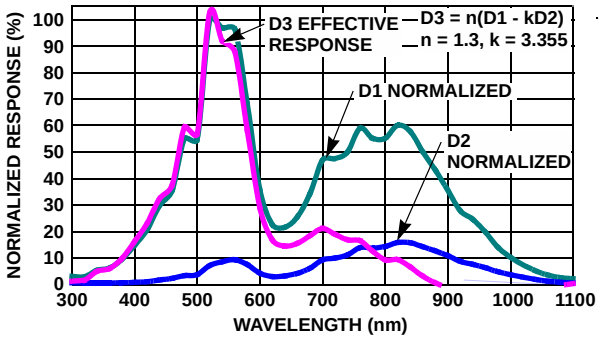


FIGURE 8. SPECTRAL RESPONSE

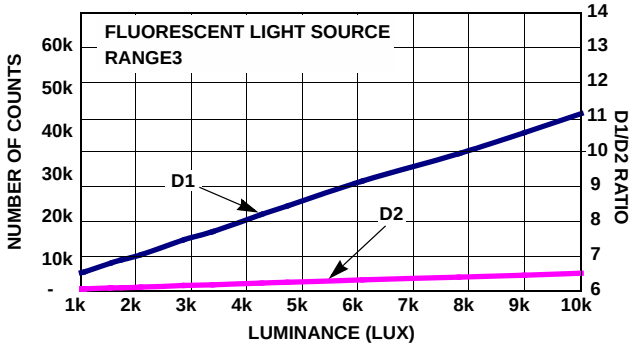


FIGURE 9. D1 AND D2 FLUORESCENT LIGHT SOURCE RESPONSE

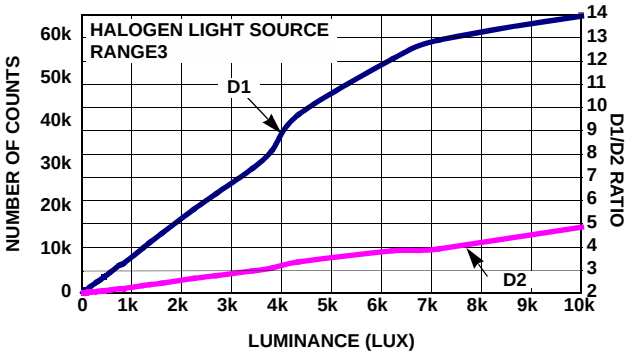


FIGURE 10. D1 AND D2 HALOGEN LIGHT SOURCE RESPONSE

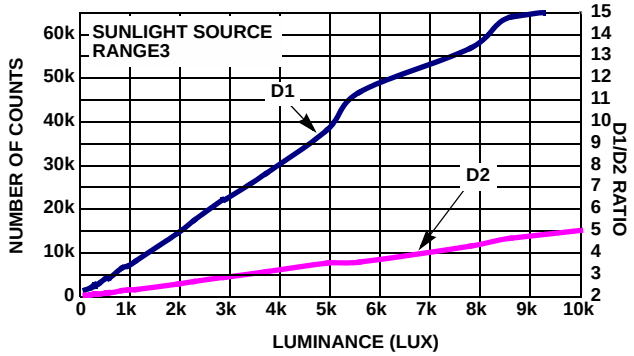


FIGURE 11. D1 AND D2 SUNLIGHT RESPONSE

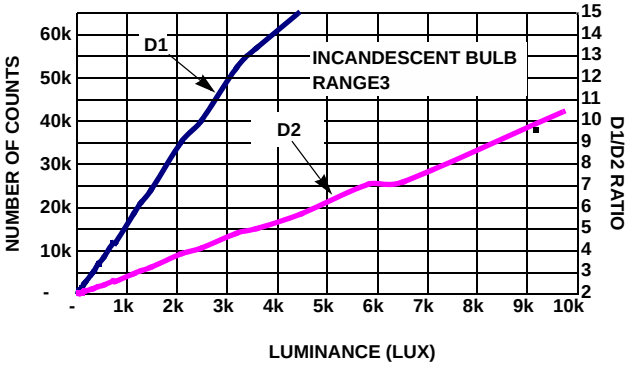


FIGURE 12. D1 AND D2 INCANDESCENT LIGHT SOURCE RESPONSE

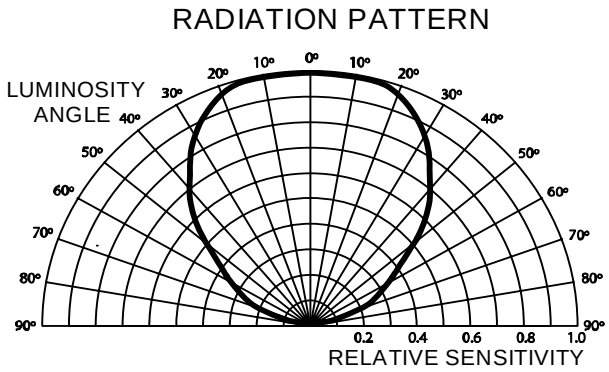


FIGURE 13. RADIATION PATTERN

Typical Performance Curves (R_{EXT} = 100kΩ) (Continued)

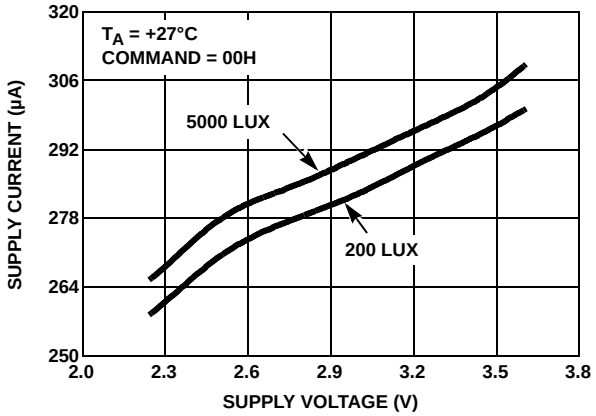


FIGURE 14. SUPPLY CURRENT vs SUPPLY VOLTAGE

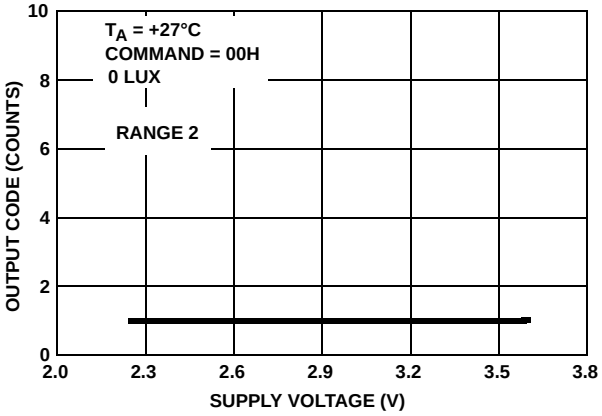


FIGURE 15. OUTPUT CODE FOR 0 LUX vs SUPPLY VOLTAGE

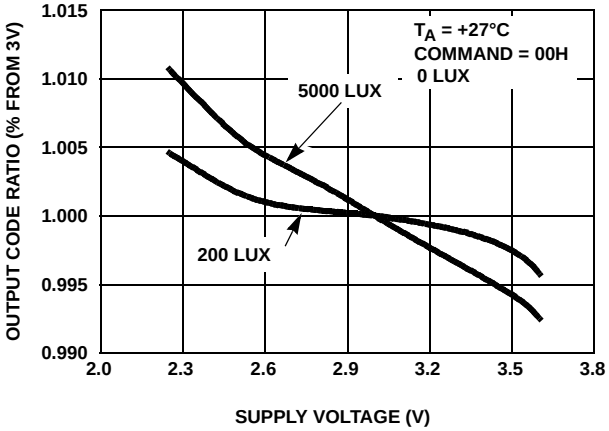


FIGURE 16. OUTPUT CODE vs SUPPLY VOLTAGE

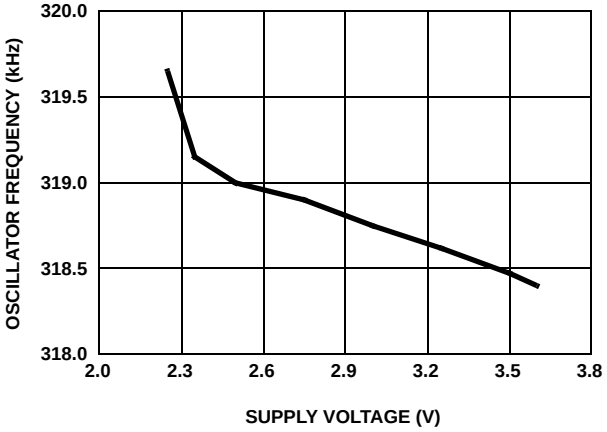


FIGURE 17. OSCILLATOR FREQUENCY vs SUPPLY VOLTAGE

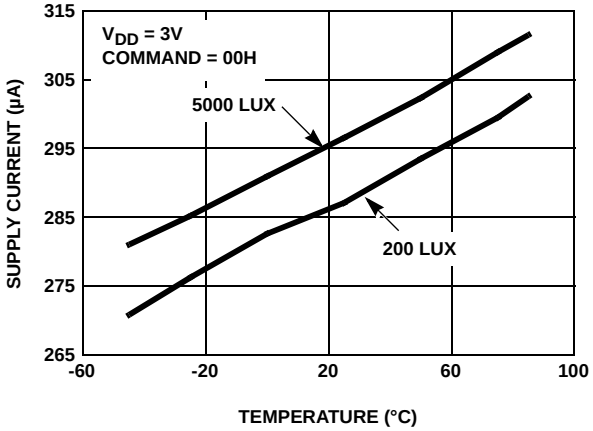


FIGURE 18. SUPPLY CURRENT vs TEMPERATURE

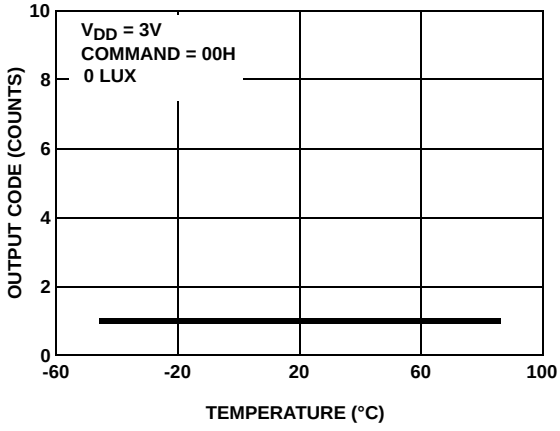


FIGURE 19. OUTPUT CODE FOR 0 LUX vs TEMPERATURE

Typical Performance Curves (R_{EXT} = 100kΩ) (Continued)

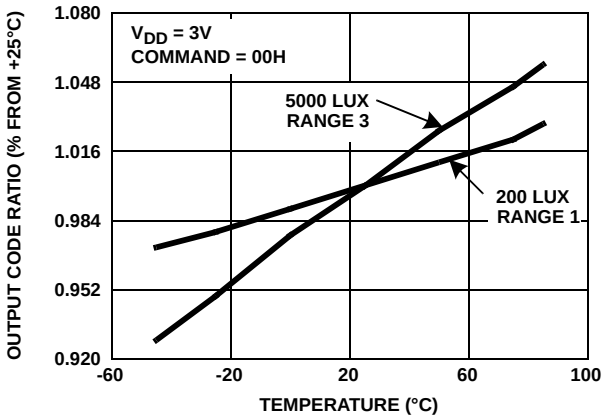


FIGURE 20. OUTPUT CODE vs TEMPERATURE

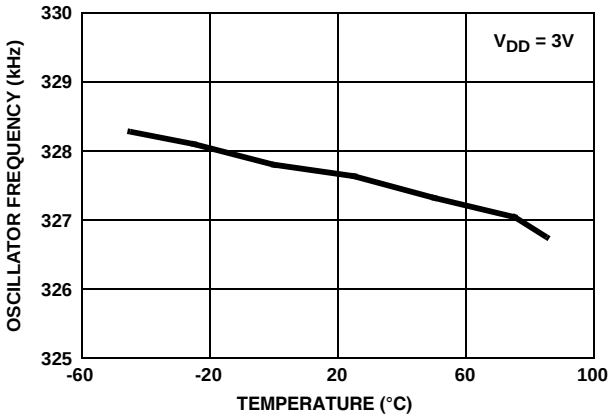
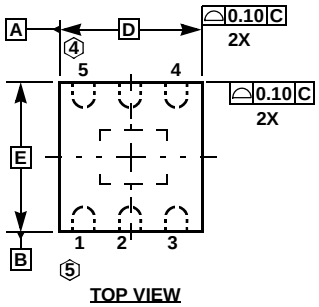
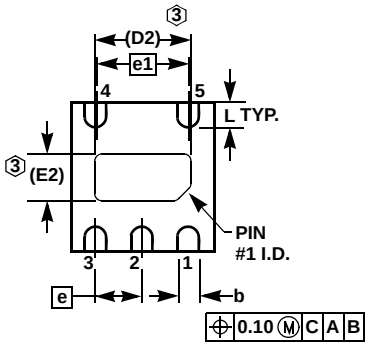
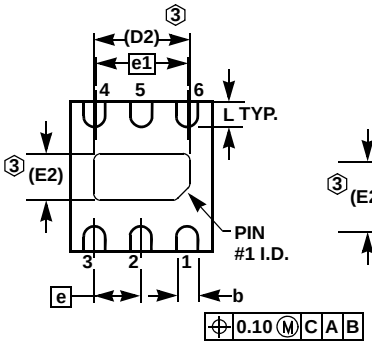


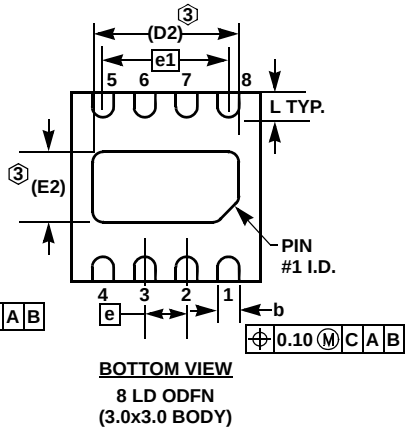
FIGURE 21. OSCILLATOR FREQUENCY vs TEMPERATURE

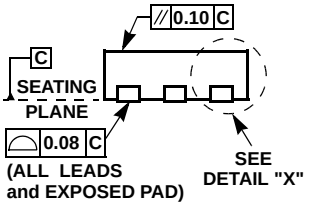
Optical Dual Flat No-Lead Family (ODFN)

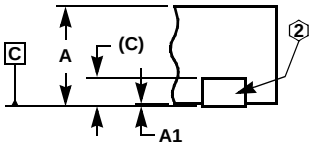












MDP0052

OPTICAL DUAL FLAT NO-LEAD FAMILY

SYMBOL	ODFN5	ODFN6	ODFN8	TOLERANCE	NOTE
A	0.70	0.70	0.70	±0.05	
A1	0.02	0.02	0.02	+0.03/-0.02	
b	0.30	0.30	0.30	±0.05	
c	0.20	0.20	0.20	Reference	2
D	2.00	2.00	3.00	Basic	
D2	1.35	1.35	2.29	Reference	3
E	2.10	2.10	3.00	Basic	
E2	0.65	0.65	1.40	Reference	3
e	0.65	0.65	0.65	Basic	
e1	1.30	1.30	1.95	Basic	
L	0.35	0.35	0.40	±0.05	

Rev. 4 5/06

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Exposed lead at side of package is a non-functional feature.
3. Dimension D2 and E2 define the size of the exposed pad.
4. ODFN 5 Ld version has no center lead (shown as dashed line).